L Number	Hits	Search Text	DB	Time stamp
1	5047	(vhdl or verilog or hdl or (hardware with	USPAT	2003/11/21 18:54
1		(definition or design) with language\$1))		
2	3878	((vhdl or verilog or hdl or (hardware with	USPAT	2003/11/21 18:56
		(definition or design) with language\$1)))		
	2617	and @ad<19990902		
6	3617	(((vhdl or verilog or hdl or (hardware	USPAT	2003/11/21 19:02
		with (definition or design) with language\$1))) and @ad<19990902) and		
		(module\$1 or sub\$1routine\$1 or header\$1 or		
		function\$1 or procedure\$1)		
7	3493	((((vhdl or verilog or hdl or (hardware	USPAT	2003/11/21 19:03
		with (definition or design) with		
		language\$1))) and @ad<19990902) and		
		(module\$1 or sub\$1routine\$1 or header\$1 or		
		function\$1 or procedure\$1)) and (initial\$3		
		or assign\$3 or set\$4 or defin\$3 or		
8	3364	<pre>pre\$1determin\$3) (((((vhdl or verilog or hdl or (hardware</pre>	USPAT	2002/11/21 10:02
	3304	with (definition or design) with	USPAI	2003/11/21 19:03
		language\$1))) and @ad<19990902) and		
		(module\$1 or sub\$1routine\$1 or header\$1 or		
		function\$1 or procedure\$1)) and (initial\$3		
		or assign\$3 or set\$4 or defin\$3 or		
		<pre>pre\$1determin\$3)) and (initial or starting</pre>		
	0.550	or first or beginning)		
9	2660	<pre>((((((vhdl or verilog or hdl or (hardware with (definition or design) with</pre>	USPAT	2003/11/21 19:04
!		language\$1))) and @ad<19990902) and		
		(module\$1 or sub\$1routine\$1 or header\$1 or		
		<pre>function\$1 or procedure\$1)) and (initial\$3</pre>		
		or assign\$3 or set\$4 or defin\$3 or		
		<pre>pre\$1determin\$3)) and (initial or starting</pre>		
		or first or beginning)) and (node\$1 or		
		signal\$1 or variable\$1 or wire\$1 or port\$1		
10	2606	or reg\$2 or register\$1) ((((((vhdl or verilog or hdl or (hardware	USPAT	2003/11/21 19:06
10	2000	with (definition or design) with	OSERI	2003/11/21 19.00
		language\$1))) and @ad<19990902) and		
		(module\$1 or sub\$1routine\$1 or header\$1 or		
		<pre>function\$1 or procedure\$1)) and (initial\$3</pre>		
		or assign\$3 or set\$4 or defin\$3 or		
		<pre>pre\$1determin\$3)) and (initial or starting</pre>		
		or first or beginning)) and (node\$1 or		
		<pre>signal\$1 or variable\$1 or wire\$1 or port\$1 or reg\$2 or register\$1)) and (condition\$1</pre>		
		or value\$1 or voltage\$1 or state\$1)		
11	1211	(((((((vhdl or verilog or hdl or	USPAT	2003/11/21 19:06
	İ	(hardware with (definition or design) with		
		language\$1))) and @ad<19990902) and		
	i	(module\$1 or sub\$1routine\$1 or header\$1 or		
i i	į	function\$1 or procedure\$1)) and (initial\$3		
		or assign\$3 or set\$4 or defin\$3 or		
		<pre>pre\$1determin\$3)) and (initial or starting or first or beginning)) and (node\$1 or</pre>		1
		signal\$1 or variable\$1 or wire\$1 or port\$1		
		or reg\$2 or register\$1)) and (condition\$1		
]	or value\$1 or voltage\$1 or state\$1)) and		
	İ	((initial or starting or first or		
	l	beginning) same (node\$1 or signal\$1 or		
		variable\$1 or wire\$1 or port\$1 or reg\$2 or		
		register\$1) same (condition\$1 or value\$1		
		or voltage\$1 or state\$1))	L	1

		1		
12	726	((((((((vhdl or verilog or hdl or (hardware with (definition or design) with language\$1))) and @ad<19990902) and	USPAT	2003/11/21 19:08
		<pre>(module\$1 or sub\$1routine\$1 or header\$1 or function\$1 or procedure\$1)) and (initial\$3 or assign\$3 or set\$4 or defin\$3 or</pre>		
		pre\$1determin\$3)) and (initial or starting or first or beginning)) and (node\$1 or		
		signal\$1 or variable\$1 or wire\$1 or port\$1 or reg\$2 or register\$1)) and (condition\$1		
		or value\$1 or voltage\$1 or state\$1)) and ((initial or starting or first or beginning) with (node\$1 or signal\$1 or		
		variable\$1 or wire\$1 or port\$1 or reg\$2 or register\$1) with (condition\$1 or value\$1		
13	510	or voltage\$1 or state\$1)) ((((((((vhdl or verilog or hdl or (hardware with (definition or design) with	USPAT	2003/11/21 19:09
	;	language\$1))) and @ad<19990902) and (module\$1 or sub\$1routine\$1 or header\$1 or		
		function\$1 or procedure\$1)) and (initial\$3 or assign\$3 or set\$4 or defin\$3 or pre\$1determin\$3)) and (initial or starting		
		or first or beginning)) and (node\$1 or signal\$1 or variable\$1 or wire\$1 or port\$1 or reg\$2 or register\$1)) and (condition\$1		
		or value\$1 or voltage\$1 or state\$1)) and ((initial or starting or first or		
		beginning) with (node\$1 or signal\$1 or variable\$1 or wire\$1 or port\$1 or reg\$2 or register\$1) with (condition\$1 or value\$1		
		or voltage\$1 or state\$1))) and ((initial\$3 or assign\$3 or set\$4 or defin\$3 or		
		<pre>pre\$1determin\$3) same ((initial or starting or first or beginning) with (node\$1 or signal\$1 or variable\$1 or</pre>		
		<pre>wire\$1 or port\$1 or reg\$2 or register\$1) with (condition\$1 or value\$1 or voltage\$1</pre>		
14	177	or state\$1))) (((((((((vhdl or verilog or hdl or (hardware with (definition or design) with	USPAT	2003/11/21 19:10
		<pre>language\$1))) and @ad<19990902) and (module\$1 or sub\$1routine\$1 or header\$1 or function\$1 or procedure\$1)) and (initial\$3</pre>		
		or assign\$3 or set\$4 or defin\$3 or pre\$1determin\$3)) and (initial or starting		
		or first or beginning)) and (node\$1 or signal\$1 or variable\$1 or wire\$1 or port\$1 or reg\$2 or register\$1)) and (condition\$1		
		or value\$1 or voltage\$1 or state\$1)) and ((initial or starting or first or		
		beginning) with (node\$1 or signal\$1 or variable\$1 or wire\$1 or port\$1 or reg\$2 or register\$1) with (condition\$1 or value\$1		
		or voltage\$1 or state\$1))) and ((initial\$3 or assign\$3 or set\$4 or defin\$3 or pre\$1determin\$3) same ((initial or		
		starting or first or beginning) with (node\$1 or signal\$1 or variable\$1 or		
		<pre>wire\$1 or port\$1 or reg\$2 or register\$1) with (condition\$1 or value\$1 or voltage\$1 or state\$1)))) and ((module\$1 or</pre>		
		<pre>sub\$1routine\$1 or header\$1 or function\$1 or procedure\$1) same ((initial\$3 or</pre>		
		assign\$3 or set\$4 or defin\$3 or pre\$1determin\$3) same ((initial or starting or first or beginning) with		
		<pre>(node\$1 or signal\$1 or variable\$1 or wire\$1 or port\$1 or reg\$2 or register\$1)</pre>		
		<pre>with (condition\$1 or value\$1 or voltage\$1 or state\$1))))</pre>		

15	16	(((((((((((vhdl or verilog or hdl or	USPAT	2003/11/21 19:12
		(hardware with (definition or design) with		
		language\$1))) and @ad<19990902) and		
		(module\$1 or sub\$1routine\$1 or header\$1 or		
		function\$1 or procedure\$1)) and (initial\$3		
	}	or assign\$3 or set\$4 or defin\$3 or		
		pre\$1determin\$3)) and (initial or starting		İ
		or first or beginning)) and (node\$1 or		
		signal\$1 or variable\$1 or wire\$1 or port\$1		
		or reg\$2 or register\$1)) and (condition\$1		
		or value\$1 or voltage\$1 or state\$1)) and		
		((initial or starting or first or		
		beginning) with (node\$1 or signal\$1 or		
		variable\$1 or wire\$1 or port\$1 or reg\$2 or		
		register\$1) with (condition\$1 or value\$1		
1		or voltage\$1 or state\$1))) and ((initial\$3		
		or assign\$3 or set\$4 or defin\$3 or		
1		pre\$1determin\$3) same ((initial or		
		starting or first or beginning) with		
		(node\$1 or signal\$1 or variable\$1 or		
		wire\$1 or port\$1 or reg\$2 or register\$1)		
		with (condition\$1 or value\$1 or voltage\$1		
		or state\$1)))) and ((module\$1 or		
		sub\$1routine\$1 or header\$1 or function\$1		
		or procedure\$1) same ((initial\$3 or		
		assign\$3 or set\$4 or defin\$3 or		
		pre\$1determin\$3) same ((initial or		
	İ	starting or first or beginning) with		
		(node\$1 or signal\$1 or variable\$1 or		
		wire\$1 or port\$1 or reg\$2 or register\$1)		
		with (condition\$1 or value\$1 or voltage\$1		
		or state\$1))))) and ((releas\$3 or free\$3)	•	
	1	same ((initial or starting or first or		
		beginning) with (node\$1 or signal\$1 or		
		variable\$1 or wire\$1 or port\$1 or reg\$2 or		
1		register\$1) with (condition\$1 or value\$1		
1		or voltage\$1 or state\$1)))		
L		or vortagest of Statest///		1